A.C.C NEWSLETTER VOL 3 ISS 5 DEC 75

Microprocessor survey

Suddenly it is all happening; new designs of 8 & even 16 bit MPU's are becoming reality, second source agreements are being signed, and prices are dropping weekly. So, for a quick gambol around the market;

INTEL

The father of it all, brought out the 4004 four bit MPU in 1971, and an improved version,the 4040, later. They are currently £13.48 & £14.23 respectively.Both MPU's are intended for fixed program, decimal applications such as cash registers and are not really suitable for general processing.

Their first 8 bit MPU, the 8008, is now available in two versions; C8008 , 20uS cycle at £20.22, and the C8008-1, 12.5uS cycle at £24.71. These can address up to 16K bytes of memory but require about 20 TTL I/C to support the basic chip.

The 8080 improved on the 8008 in four basic ways; first it used a 40 pin package, reducing the number of support pack needed,cycle time was reduced to 2uS, addressing capability was increased to 65k bytes, and the instruction set was enhanced, particularly in the addition of a main memory stack and instructions for handling it.There are a number of versions available, the latest of which (8080A) has TTL drive capability and is now £40.13.

A kit, the MCS-80/C, is available for £96.80 and includes 14 I/C; MPU, parallel & serial programmable interface units, 256 bytes of RAM, 1K bytes EPROM.

Texas Instruments now sell a second source, the TMS 8080.

The 8008/8080 are probably the most widely used MPU at present but, probably because they were the first, suffer from the disadvantages of a rather 'bitty' instruction set and the need for multiple power rails (+12, +5 & -5V)

F8

Produced by Fairchild and Mostek, this 8 bit MPU is designed to give a minimum package solution to simple applications e.g. traffic light controllers. The CPU chip includes a clock generator, 64 byte RAM, two 8 bit I/O ports, so a minimum system can be made with only two chips (CPU & ROM) and a timing crystal.2uS cycle time, 64k byte addressing range, 72 instructions. +5 & +12V supplies. Fairchild version (3850 DC) £54.60 from Semiconductor Specialists.

MOSTEK 5065P

Another 8 bit MPU, 32k bytes addressing range, TTL compatible inputs & outputs, 10uS cycle time. +5 -5 -12 V supplies. £34.80 from Semiconductor Specialists.

Signetics 2650

One of the more recent 8 bit devices, this MPU requires only one +5V supply, gives a 2.4uS cycle time and can be used as a static device for ease of debugging.It has four on-chip registers which can be used as truly general purpose registers. Relative, immediate, absolute, indirect, indexed and register addressing modes are provided, and it can handle up to 32k bytes of memory.£99.00 from Semiconductor Specialists.

MOS Technology 65**

A new range based on the 6800 but with modifications such as; two real index registers,two forms of indirect addressing,fast decimal arithmetic. Somewhat faster than the 6800 or 8080 in typical operations, despite the improvements the 6501 is said to be plug compatible with the 6800. The 6502 is similar but with an internal clock circuit.The 6501 & 2 use a 40 pin package and can address 65k bytes of memory, the 6503/4/5 are in 28 pin packs and give various combinations of 4 or 8k addressing and one or two interrupt lines.Only available from the States, big attraction is that the 1 off price is not much above the 100 up price. MCS6502 is $25, others are $20 !

6800

Introduced by Motorola, second-sourced by AMI, this device looks like becoming the industry standard 8 bit MPU. 40 pin package, TTL compatible (including single +5V supply). Two accumulators, index register, stack pointer.64k bytes addressing range. 3 state data bus.£41.40 from Semiconductor Specialists, and falling.

SC/MP

An 8 bit device from National Semiconductor, just released, haven't much information as yet but we understand that it is intended as a very low cost easy to use MPU for applications such as electronic games, fuel injection units.

RCA CDP 1800

This is rather out of the ordinary; a two-chip COSMOS 8 bit microprocessor with a very simple instruction set. All instructions are single byte with equal instruction times. 16 16 bit registers can all be used as program counters, data pointers or for data storage. Cheapest version at £24 from Semiconductor Specialists is the 2 chip set CDP 1801 CD.

6100

Designed by Intersil & second sourced by Harris, this is a 12 bit CMOS MPU with the PDP-8 instruction set. A single supply in the range 4 - 11V the typical operating power is 10mW and the memory to accumulator add time is 5uS. Available from Semiconductor Specialists as the IM6100CDL for £31.20.

PACE

The new National Semiconductor 16 bit single chip MPU is a development from their previous IMP 16 bit multi-chip MPU sets.It uses 16 bit instruction words and can handle 8 or 16 bit data.4 accumulators and a 10 word stack are provided on the chip. 10uS typical instruction time. +5 & -12V supplies. £120.

1600

The new General Instrument 16 bit single chip MPU CP1600 @ £47.00 from Semiconductor Specialists. We don't have any other details except that it is said to look like the PDP-11.

9900

From Texas Instruments, a single chip 16 bit MPU, at the moment they are not selling it as an individual component, but will probably do so some time.

F100L

Promised for next year this is a 16 bit single chip MPU using CDI to achieve a 10MHz clock rate. To be made by Ferranti.

CRAMERKITS

A lot of microprocessor 'kits' are available from varying sources, including the previously mentioned Intel ones. Cramer Electronics are offering some including the MEK6800D1 for £85. This gives you a 6800L MPU, 256 bytes RAM, 2 6820L peripheral interface adaptors, a 6850L asynchronous communications interface adaptor, PC board and manuals.

IN THIS ISSUE

MICROCOMPUTERS

A number of fairly cheap single board processors (usually including memory and perhaps limited I/O) appearing now. Among them are;

990/4

From Texas Instruments, using the 9900 MPU. £228 with 512 bytes of memory, £318 with 8k bytes.

GA-16/110

16 bit machine from General Automation with 1k words of memory. £531. Software compatible with the SPC-16 machines.

LSI-11

DEC's single board PDP-11. £371 with 4k words of RAM.

ADDRESSES

Intel devices from Rapid Recall, 9 Betterton St., London WC2H 9BS tel 01 379 6741

Semiconductor Specialists ; Premier House, Fairfield Rd., Yiewsley, Middlesex. tel West Drayton 46415

MOS Technology Inc. ; Valley Forge Corporate Centre 950 Rittenhouse Road. Norristown. PA 19401 USA

Motorola also from Semicomps ; Wellington Road, St Albans Herts

National Semiconductor (UK) Ltd ;19 Goldington Rd., Bedford MK40 3LF tel 0234 211262

Texas Instruments ; tel Bedford 67466

Cramer Components Ltd. ; 16 Uxbridge Rd., Ealing, London W5 2BP tel 01 579 3001

PRICES

Quoted above are based on the latest available information that we have but are not necessarily up to data. All are without VAT, P&P etc., and are 'one off' for the MPU chips but 'more than 50, OEM,' for the Microcomputer boards.

LETTERS

SYNTH

I am very interested in computer hardware systems and in electronics, particularly with a view to building an electronic synthesiser (digital !) based on any suitable current MPU (I am particularly concerned that the system should satisfy any 'serious' musician !) If any of your members are particularly involved/intrigued/interested in the above, or similar applications, I will be grateful if they would get in touch with me.

M Kaleel YWCA International House
Penn Road Wolverhampton WV3 0DW

SHOP !

I have an 80 column hand punch in good working condition which I would like to exchange or part exchange for a teletype terminal or similar equipment.

G Bell 55 Belvedere Rd Hessle North Humberside
Tel 0482 645724

Wanted : 1 Terminal ITEL 500 with MCT 500 processor interface EBDIC code, paper tape punch & reader.

G Depre V. Beauduinstraat 91
B 3300 Tienen BELGIUM

PASCAL

When Algol 60 was produced in the 60's, a gentleman by the name of Nicklaus Wirth realised that, although it was good, it still left some things to be desired. Along with a group of other people he set about designing a better language. For reasons too long and complicated to go into here they split up. Wirth went on to produce Pascal, and the others went on to produce Algol 68. The algorithmic statements of Pascal are based on the principles and notation of Algol 60, but the data structures of Pascal are much more general than those of Algol 60. It permits hierarchal structuring of data and program, extensive error checking at compile time, and production of efficient machine code on present computers. If you are familiar with Algol 60, you will find it easy to adopt Pascal as your programming tool.

Refs;

NIKLAUS WIRTH, The Programming Language Pascal
ACTA INFORMATICA 1/1 May 71 pp 35-63

NIKLAUS WIRTH, Design of a Pascal Compiler
Software Practice & Experience 1/4 1971

PER BRINCH-HANSEN, Operating System Principles
Prentice Hall 1973 pp 32-42

P Rutherford

BOOKS

I recommend the following books (not necessarily to be bought but worth reading)

INTRODUCTION TO COMPUTER TECHNOLOGY
by L Nashelsky Wiley 1972 £4.70

DISPLAYS (Conference at Loughborough Univ Sep 71)
IEE conference publication No 80

ELECTRONIC COMPUTER MEMORY TECHNOLOGY
W Riley (ed) McGraw Hill 1971

The latter book on memories is especially worth reading (even though written in '71 it has some information on the new SOS technology)

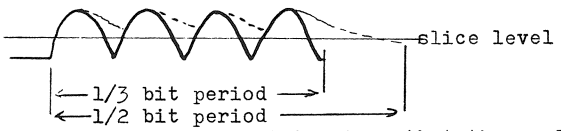
P D Maddison

HITS TV & CHIPS

I have a few comments to make on various topics;

Cassette Data Storage

A standard system for using audio cassette recorders for data storage is a great idea. The Hobbyist Interchange System fills me with some doubts though. (probably due to not reading the complete original article !) The system seems fine up to the point where 2kHz tone is used as a 'mark' signal. In fact apart from that it sounds much like the DEC system on the little I know about it. But the way the diagramms were drawn suggests that someone hadn't realised how few cycles of 2kHz occur within the bit period. In fact the number is 5½. One third of this is 1 and 5/6 cycles. If rectified this becomes 3 and 2/3 half cycles. In order that the bit can be read as a 1 or a 0 the rectifier smoothing circuit time constant must be chosen to decay to the slicing level in less than 1.67 half cycles but not to do this between half cycles.

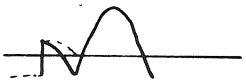


This is just about possible given that the amplitude of the sine wave is known (and slicing levels chosen accordingly, requiring some form of AGC) and that the bit rate really doesn't change as this would modify the time constant required (this rather defeats the advantage of the coding scheme).

However a further problem is that since an incomplete number of whole cycles is transmitted a DC offset could develop and throw out the circuit.

Unless both positive and negative peaks were clamped. None of this is impossible but the circuit is by no means simple or foolproof.

Note also that if a sine wave is commenced part way through it may give a false bit in spite of hysteresis & carefully chosen levels.



Low pass filters can add delays so the design of these must be carefully considered.

Couldn't some practical work be done to choose system parameters ? For example a higher frequency than 2 kHz would simplify things (how about 5kHz ?) The 1/3 & 2/3 bit periods could be modified to $\frac{1}{4}$ & $\frac{3}{4}$. The system could require that an integral number of complete cycles was transmitted to reduce DC offset problems.If we are to have a club standard it should be a reliable proven one.

Telewriter

Such a device is the only answer I can see to a cheap reliable teletype substitute. The second hand teletype market is bound to be sporadic and fairly costly and the machines of dubious reliability. Although I haven't seen the article you refer to I think it is worth pointing out that the imminence of Teletext / Viewdata is going to make the TV teletype substitute a reality for anyone who wants it. Teletext is the system for transmitting data in the frame blanking interval of a TV picture and displaying on the screen (e.g. CEEFAX, ORACLE) Viewdata is the BPO system for transmitting selected information down a telephone line and displaying it on the TV screen. The systems are display format compatible and their success depends on manufacturers producing a cheap set of chips (£30 - £50) to produce the display within a couple of years. Manufacturers are unlikely to overlook the VDU potential in their chip desigh and my feeling is that they will produce facilities for a rolling page (note this is not a requirement in Viewdata or Teletext) The immediate value of the information is to prepare us for the possibility of the chips being available and to allow us to choose a display format in our present endevours which will not have to be changed if we made a Teletext chip based display. Briefly the Teletext display is 24 rows of 40 characters. The character set is almost the same as ASCII but with a few national options and other mods due to the difference between TV screens and teletypes (it is hard to underline on a TV screen) and also for the BPO requirements for Viewdata.

Microprocessor Chips

The Intersil IM6100 is a microprocessor which is software compatible with the PDP8E. One off price is £88.50. It has facilities for connecting a control panel without disturbing the operation of the processor. The chip uses static logic and so can be clocked as slowly as required for debugging. Unfortunately the parallel interface chip is not software compatible with the PDP8E and therefore although a simple hardware system could be built, if it is required to use the DEC software a special Teletype interface has to be built using quite a lot of chips. I was very interested in this system as I thought it might offer a cheap route to a 4K PDP8E so that I could run something like FOCAL without having to write it, but it still seems a bit expensive.

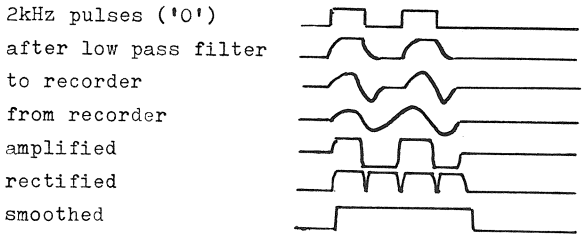
A cheaper solution to get into would appear to be the Motorola M6800 ; it looks much like the WB in organisation, and a kit is being offered of a CPU, 2 off 128 x 8 static RAM, one peripheral interface adaptor, and a 1024 x 8 ROM containing some simple keyboard / cassette / paper tape control programs plus a PCB, all for £85 (GDS Sales Ltd).

P Crowe

**** about the HITS ; think the system is in fact workable & the problems are due to the bad explanation I gave. So, after re-reading the original article may I add the following;

2kHz was chosen as a frequency which would work with any cassette machine; it may be pessimistic and it was in fact suggested that higher frequencies could be used for private use; however since 2kHz appears to be the standard lets stick to it.

The recording technique shown used 250uS pulses at a 2kHz rate. These were passed through two CR filters; one low pass (470pF 100k) then a high pass (0.47uF 1k) before being recorded. This,with the recorder frequency response, gives a rough sine wave with, as you have pointed out, an integral number of cycles. They used two pulses (2 cycles) to record a '0'; slightly longer than an exact one third (I tend to agree with your choice of $\frac{1}{4}$ & $\frac{1}{2}$, but think the thing would work with their figures, and again, as it is a proposed standard, lets stick to it). The basic trick, which I didn't explain, is to amplify the received signal enough so that it is almost a square wave before it is rectified. This means that the rectifier output is 'high' for most of the time when receiving a pulse train, so the smoothing circuit time constant can be kept short (they used 0.1 mS).Waveforms below;



Would be interested to hear from anyone who is working on suitable hard/soft ware.

m lord

WB

I wonder if you have considered battery backup for the Weeny-Bitter memory. Assuming that the 2101's will hold data down to 2.8V supply, a single 126 battery should give 50 Hrs life for moving the machine around. If P5101-8's could be afforded at £8.11 each a 126 battery should hold the memory for well over one year and you would not end up leaving the WB permanently on.

Data on 5101-8 significant differences from 2101 (it is pin compatible);

Ambient temperature under bias	10 to 80°C
Voltage any pin to ground	-0.3V to Vcc +0.3V
Operating current	15mA typ, 30mA max outputs open
Standby current 50uA	Vin=0 to Vcc except; CE2 less than 0.2V.
Access time	800nS max
$\overline{CE1}$ to output	800nS max
CE2 to output	850nS max

For the necessary supply diodes for a battery backup system I would suggest trying medium current germanium transistors such as the OC72 or AC128 with their collectors tied to base. Normal silicon diodes may give too high a voltage drop especially with the 5101 (see spec above).

Although I like the WB I reckon the pin count is too high for my capability so I will probably go for an 8080. Present line up is;

8080A	£54	1.9mA sink on all outputs for the A version
8224	£ 6.90	Clock generator / driver.
8228	£ 8.11	System controller, 8mA sink data bus buffer + single interrupt Vector.
8111 x 2	£ 6.38	256 x 8 RAM
8205	£ 2.12	1 out of 8 decoder
8255	£12.68	3 x 8 bit programmable I/O ports
5101-8 x 2	£16.22	ROM plug in board with battery back up & seperate switch loader

Have you any advice on EPROM erasers - suitable bulbs and their circuits and suppliers - use of arc welders etc. £98 for Rapid Recall's is a bit much but may be OK for a shared expense if some other members are interested. The 8704 512 x 8 bit EPROM looks possible for a simple switch programmer and I think its price should drop from its present £33.76.

Is there any way of getting at the Intel 8080 library other than by paying them £50 or by giving them a program which is difficult without a computer to develop it on ?

J D Owen

Some points on the WB;

1) The 2101 memories offered by Rapid Recall at £3.04 are the 1uS Access time version. Your notes on WB state that the Read & Write lines are held up for a minimum of 0.5uS ?

2) Whilst a signal is generated on the address board to inform the control that an address ≤ 003 is on the bus, there is no logic to decode the lower two address lines and as these lines are not connected to the control I cannot see how it can distinguish.

3) Members may be interested to hear of the following method of overcoming the restricted memory size of the WB-1 in advance of enhancement to WB-2

An extension memory could be constructed as an I/O unit. It would use three I/O ports;

1 EMA Extension Memory Address, write only
2 EMR Extension Memory Read, read only
3 EMW Extension Memory Write, write only

Access would be by software as follows

```
READ                    WRITE
MOV #N  EMA             MOV #N  EMA
MOV EMR A               MOV A   EMW
```

where N is the address required.

Programms could not be executed from the extension memory but they could be stored there and copied to main store for execution. If the extension was constructed such that its address reg was a counter that automatically incremented by one on every R/W access the following program would copy a 'page' of program from extension to main mem and then enter it . (I have used ↓ to represent a labelled data or address byte)

```
FETCH:  MOV ↓ COUNT     ; load COUNT with length of
LEN:    #Ø              ; page - 1
        MOV ↓ A         ; load A with address of
PAD:    #Ø              ; Byte 1 in extension
        MOV A EMA       ; Send to extension
        MOV ↓ A         ; load A with address in
SAD:    #Ø              ; main store of first byte
        MOV A TAD       ; send to byte labelled TAD
        MOV A GAD       ; send to byte labelled GAD
NEXT:   MOV EMW A       ; read byte from extension
        MOV A ↓         ; send to main memory
TAD:    #Ø
        INC TAD         ; increment main mem addr
        DEC COUNT       ; decrement count
        JNZ NEXT        ; loop if not zero
        GTO ↓           ; jump to first byte of
GAD:    #Ø              ; program
```

This routine would be called for example by the following sequence;

```
MOV  #9 LEN     (all numbers in decimal)
MOV  #23Ø PAD
MOV  #64 SAD
GTO  FETCH
```

1Ø bytes would be brought from the extension at address 23Ø→ and stored in main memory at 64→ control would then be transferred to address 64.

I hope the above will prove useful to someone.

T Connell

***** The timing given in last issue was provisional and really intended to help anyone trying to design I/O circuits; the actual times for the WB-1 are in fact longer as detailed in this issue, but there is always the possibility of using a faster memory, in which case it would be worth keeping to the 0.5uS figure for I/O design.

Sorry about the address line drop-off. the AØ & A1 lines should have been extended to the control unit.

mike lord.

COMPUTER DATING

The algorithm will give the day of the week of any date, and I believe it to be the first such published algorithm to be fully corrected both for the 1752 hiatus and for the fact that years ending in 00 are not leap years unless the year as a whole is exactly divisible by 400. I find this algorithm very useful on my pocket calculator, as it eliminates the need for diaries, calendars etc.

In English, the algorithm is;

If the year is negative (BC) add a multiple of 400 to give an equivalent positive year.

Take all except the last two digits of the year and divide by 4, noting the remainder.

If the required date is up to 2/9/1752, use the figure given by Table A, column 1, as your working figure; if the date is 14/9/1752 onward use the figure in column 2. To this working figure add the last two digits of the year.

Divide the last two digits of the year by 4, integerise the result, and add this to your working figure. Look up the appropriate month figure in Table B and add this to your working figure.

Add the day of the month to the result. Finally divide by 7, again noting the remainder. Given this information look up the day of the week in table C. For convenience to calculator users I have also included the figure after the decimal point, in brackets, in this table.

For example : 4 July 1776
The 'century' digits are 17, which divided by 4 leave a remainder of 1. According to Table A the appropriate working fogure is 4.
To this add 76, giving 80.
76 divided by 4 is 19, giving a total so far of 99.
The month figure for July is 0, leaving the total unchanged.
Finally I add 4, giving 103, and divide by 7.
The calculator display now reads 14.714285 ; according to table C, .7 corresponds to Thursday.
So now you know the exact date of American Independance Day.

I would like to hear, via the newsletter, from anyone who has any other calculator algorithms. Any one know a good random number generator for calculator use ?

R Baker

TABLE A

Rem	Working figure 1	2
0	3	6
1	1	4
2	6	2
3	4	0

TABLE B

JAN 1 (0 in leap year)
FEB 4 (3 in leap year)
MAR 4
APR 0
MAY 2
JUN 5
JUL 0
AUG 3
SEP 6
OCT 1
NOV 4
DEC 6

TABLE C

SUN 1 (.1)
MON 2 (.2)
TUE 3 (.4)
WED 4 (.5)
THU 5 (.7)
FRI 6 (.8)
SAT 0 (.0)

BOOK

A book really worth reading is;
DIGITAL SYSTEMS : HARDWARE ORGANISATION AND DESIGN by Frederick Hill & Gerald R Peterson
Publishers ; Wiley & Son ISBN 0-471-39605-2
The book covers most important points of the ALU, CPU plus.

N Trewartha

SYNTH 2

I have recently completed construction of the ETI 4600 Synthesiser and am now considering building a programming device / sequencer. Do you know of someone who could offer assistance ?
P Dawson 11 Claremont Gdns., Whitley Bay, Tyne & Wear NE26 3SF

YORKSHIRE LEO

Sheffield University have obtained a LEO III/s with sufficient peripherals to form a working system and are now looking for people to reassemble the machine and get it working. If you can help contact S Bennett, Dept of Control Engineering, The University, Mappin St, Sheffield.

SCHOOL COMPUTER

Imberhome School, East Grinstead, have been given a System 4-30 computer.

ED'S BIT

Dramatic increase in membership following the publicity in Wireless World and ETI; now nearly 350 members ! Thank you Jon Aslett.

One immediate advantage of this increase- now we won't have to increase the subscription for the next year (next year is from April 1, still one further issue of this volume to go). Welcome to all new members - hope you stay with us - and can I persuade some of you to contribute pieces to the newsletter ?

The WB project seems to have caught peoples' imagination - could we have some thoughts on a possible follow up for next year?.

Finally, may I extend my best wishes for a happy and prosperous New Year to all our members.

mike lord

* THE WEENY-BITTER *

HARDWARE PART 2

Changes so far . . .

As pointed out elsewhere in this issue, the AO and A1 line also go to the control unit.

On the address logic circuit diagram (page 14 of the last issue) the reset inputs to the 74193 counters (pin 14) should be connected to OV.

The 'STOP' button shown on page 8 of issue 4 is not needed for the basic WB - the machine can be stopped by turning the function select switch to the 'SS' position (Single Step).

Indirect addressing has seemed so attractive a feature that it has been added to the control logic in this issue (addressing mode 1). This may simplify T Connell's extended memory routine on page 4.

Otherwise everything seems OK.

Points from the Seminar;

Speed; the time varies according to the type of instruction being performed but is of the order of 10uS per instruction.

Expandability; Upgrading the basic machine to the WB-2 basically involves (apart from adding more memory) adding more bits to the MA & PC regs to handle the extended memory and altering the control unit. The best way of doing this has not yet been established - we could have more of the same type of logic or we could scrap most of it and go in for a microprogrammed approach, which I think at the moment to be the best way. The Arithmetic Unit would be unchanged.

Does it work; as far as I know, one has been built and quickly tested (this newsletter is being produced in a rush because of the immanence of Xmas holidays and the printer's close-down) but because they weren't available in time the 2101's were not actually used for the memory but TTL RAM's substituted.

CONTROL UNIT

This is the nasty, messy, part of the machine. The basic problem is to provide a sequence of pulses with the right timing and in the right order to the various control lines (SRO ZIN CA MA etc.) so that information is manipulated as required.

We have 9 basic types of instruction (see table) some of which can be modified by the addressing mode bit, and in addition we must allow for some special functions initiated from the operator control panel.

Taking the control panel first, and referring to the sketch on page 8 of Iss 4, then we have;

A switch register made up of 8 toggle switches. This is used to set the program counter to a specific address under operator control, as a way of loading data into the machine, again under manual control, and the state of the switches can be interrogated by a running program with a

```
        MOV  #1 A
or      TST  #1
or      CMP  #D  #1
or      BIT  #D  #1     instruction
```

8 data lamps which are connected to the DATA BUS. When the machine is running information on the bus will be changing too fast to be visible but the control circuits switch the contents of the A reg in the arithmetic unit onto the bus whenever the machine is halted.

8 address lamps connected to the ADDRESS BUS. Again this information changes too fast to be visible when the machine is running but the control circuits connect the Program Counter to the bus when halted.

A 'C' lamp to show the current state of the C bit register. (Z & P lamps are not provided)

A 'Run' lamp that is lit when the machine is not halted.Note, a long 'WAIT' from a very slow peripheral device will make the lamp go out.

A rotary Function switch. The functions are;

RUN In this position the machine, once started, will execute the user's program until a HLT instruction is encountered.

SS 'Single Step'. In this position the machine will only execute a single instruction each time the GO button is pressed. This allows us to step through the program , looking at the A reg after each step. Note that the address shown on the address lamps after each step is the address of the next instruction to be executed, rather than the address of the one just done.

LOAD PC In this position operation of the GO button will load the program counter with the address set up on the switch register. This address is then shown on the address lamps.

EX 'Examine'. When the switch is in this position operation of the GO button will cause the contents of the memory location pointed to by the program counter to be read into the A reg of the arithmetic unit, then the program counter is incremented to point at the next location. Note that after each operation of the GO button the data which was read is displayed on the data lamps, and the address lamps will be showing the address of the next location - the one after that containing the displayed data. Repeated operation of the GO button allows you to read data from any number of sequential locations, without having to keep on loading their address.

DEP 'Deposit'. When the switch is in this position operation of the GO button stores the data set up on the switch reg into the memory location pointed to by the program counter, then the program counter is incremented. This data transfer does not go through the arithmetic unit so the A register, and the data display, remain unchanged. Note that after operation of the GO button the address lamps are showing the location after that into which the data was deposited. As with EX, repeated operation of the GO button allows you to load data into any number of sequential locations.

OPERATION OF THE CONTROL CIRCUITS.

12 'states' (S1 to S12) have been assigned and the control circuit steps through these according to the flow chart.

S1 is the HALT state, in which the unit clock is stopped . Operation of the GO button restarts the clock and moves you to S2 or S3 according to the setting of the function switch. Once it has got to S3, the machine runs continuously, looping through the higher numbered states as determined by the instruction and back through S3 until a HLT is encountered.

S3 reads the first word of the instruction from the memory location pointed to by the program counter into I (instruction reg), then increments the program counter. If it is not a miscellaneous instruction or one of the form OP A, the machine goes to S5 which reads the second instruction word into the A,B & M registers then increments the program counter. S6 reads the third word of the OP #D X type of instruction into the M reg.

S7 & S 8 get the correct operand address for an indirect addressing mode instruction.

S10 reads the only operand of a single operand type instruction, or the second operand of a two operand type, into the A reg. (Q is defined thus)

S11 puts the other operand of a two operand instruction of the form OP A X or OP X A into the B reg (the immediate mode data byte for an OP #D type has already been read into the B reg at S5)

S12 takes the result from the arithmetic unit and writes it into the Accumulator (mem location 0) or mem location X as appropriate.

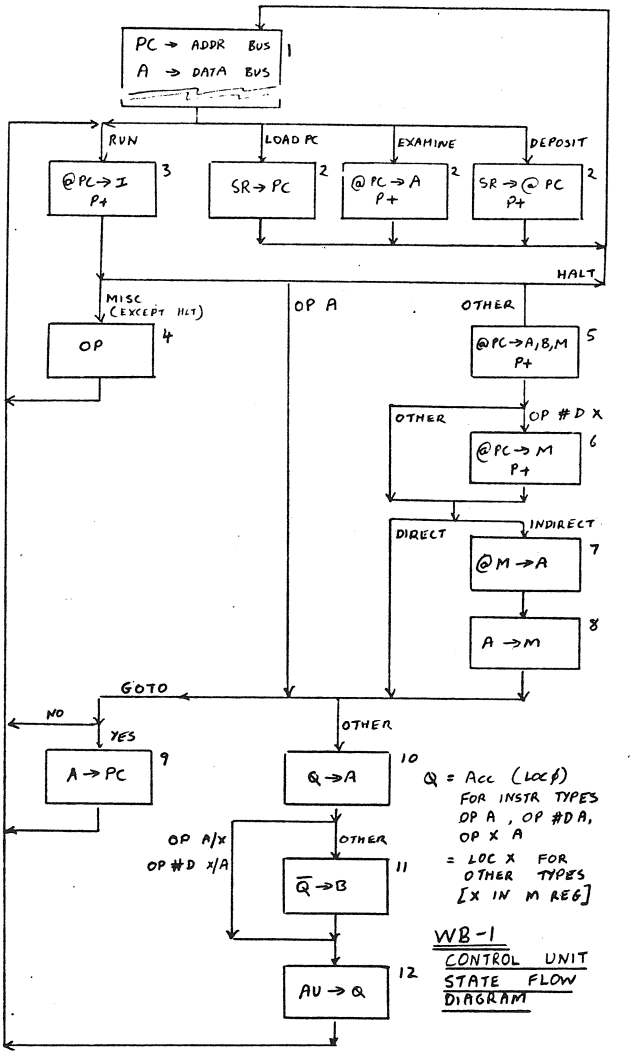
Page 7 gives the circuits used to generate the S pulses.

The basic timing is derived from two 74121 monostables X1 & X2. The 100uF, 10k circuit connected to X4 ensures an orderly start-up on switch on of the machine power supply. Pulling the WAIT line to ground freezes the clock circuit with CL (X2 pin 1) high, and turns off the RUN lamp. The CL clock waveform is inverted, delayed slightly, and buffered in X5,4 & 11 and is then used to clock a long shift register (X12,13,7,8,9,10) made from D type flip-flops (7474's). These are arranged so that all except one of their 'Q' outputs are at 0; and kept this way by the reset pulse applied to all of them except the S1 one whenever the machine is in the S1 state (from X11 pin 3).

BASIC INSTRUCTION TYPES

op code (octal)	mnemonic	operation
00*	Misc (HLT, CLC etc)	
10*	OPa A	Acc := OPa . Acc
11* DDD	OPb #D A	Acc := Acc . OPb . #D
n2* XXX	OPb X A	Acc := Acc . OPb . X
n3* XXX	G X	Go to X
n4* XXX	OPa X	X := OPa . X
n5* DDD XXX	OPb #D X	X := X . OPb . #D
n6* XXX	OPb A X	X := X . OPb . Acc
n7* XXX	J X	Jump to subroutine X

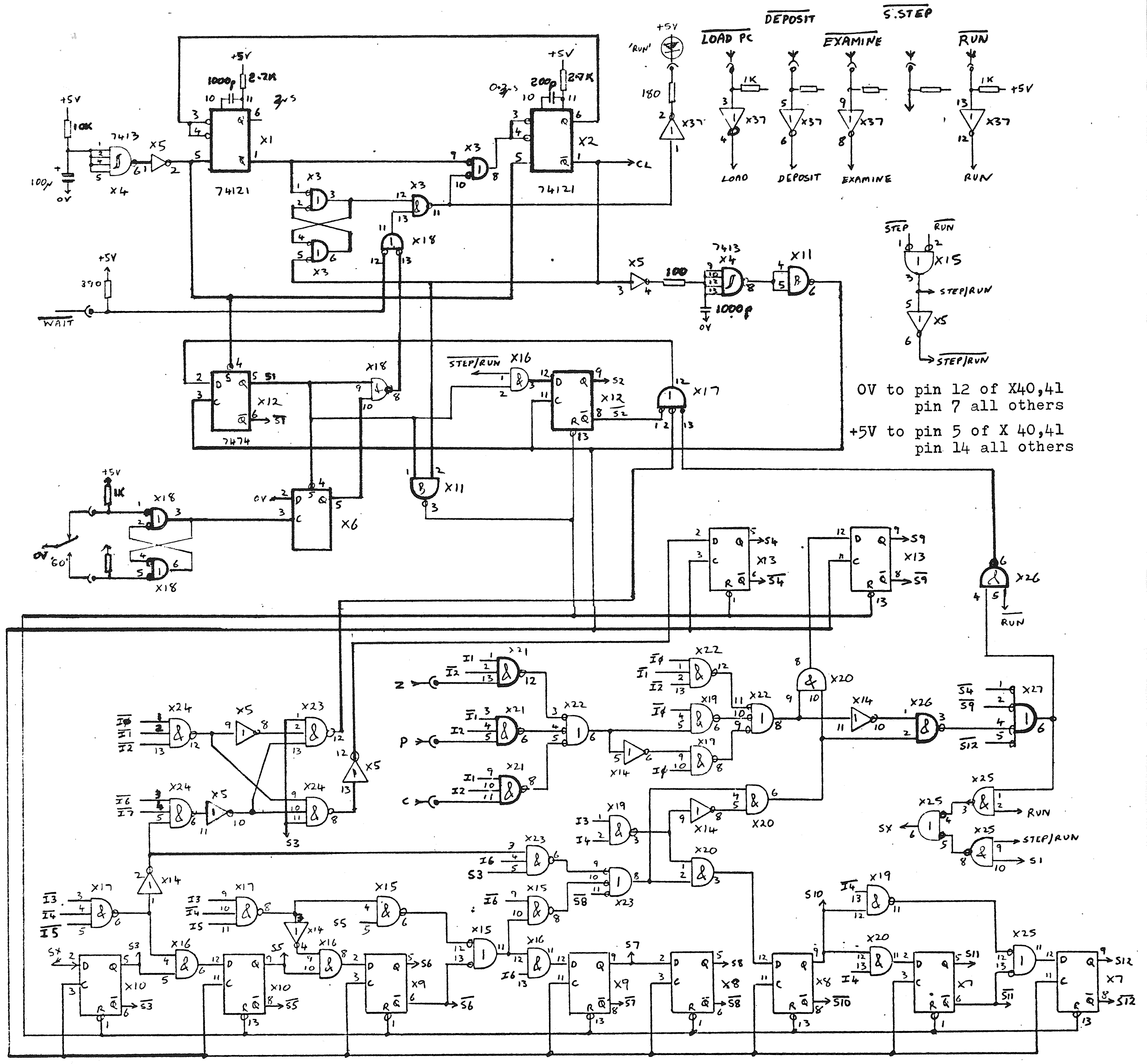
notes; * defines op
n defines addressing mode
OPa = single operand instructions (eg CLA)
OPb = double " " (eg MOV)



Page 8 shows the instruction register and the miscellaneous gating circuits used to sort out the control signals (SRO PCA etc) from the S lines and the actual instruction (I).

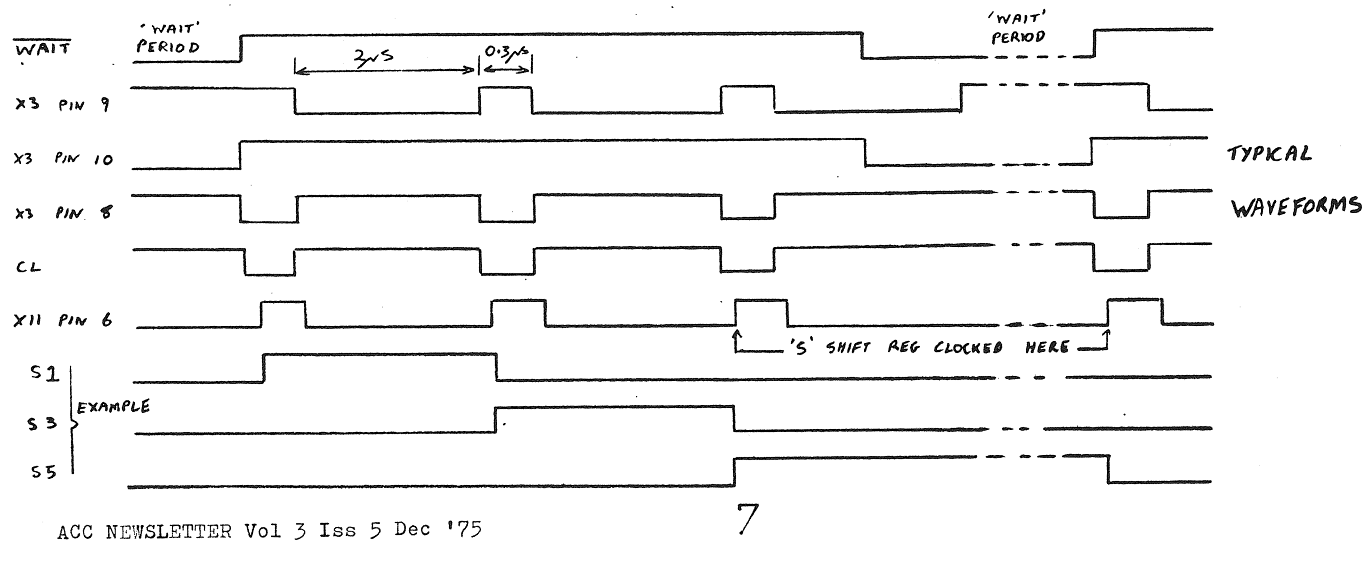
The control unit can be tested fairly easily by removing all of the connections from pin 1 of X2, and connecting them instead to pin 6 of X18. The unit will then step on one state every time the GO button is pressed.

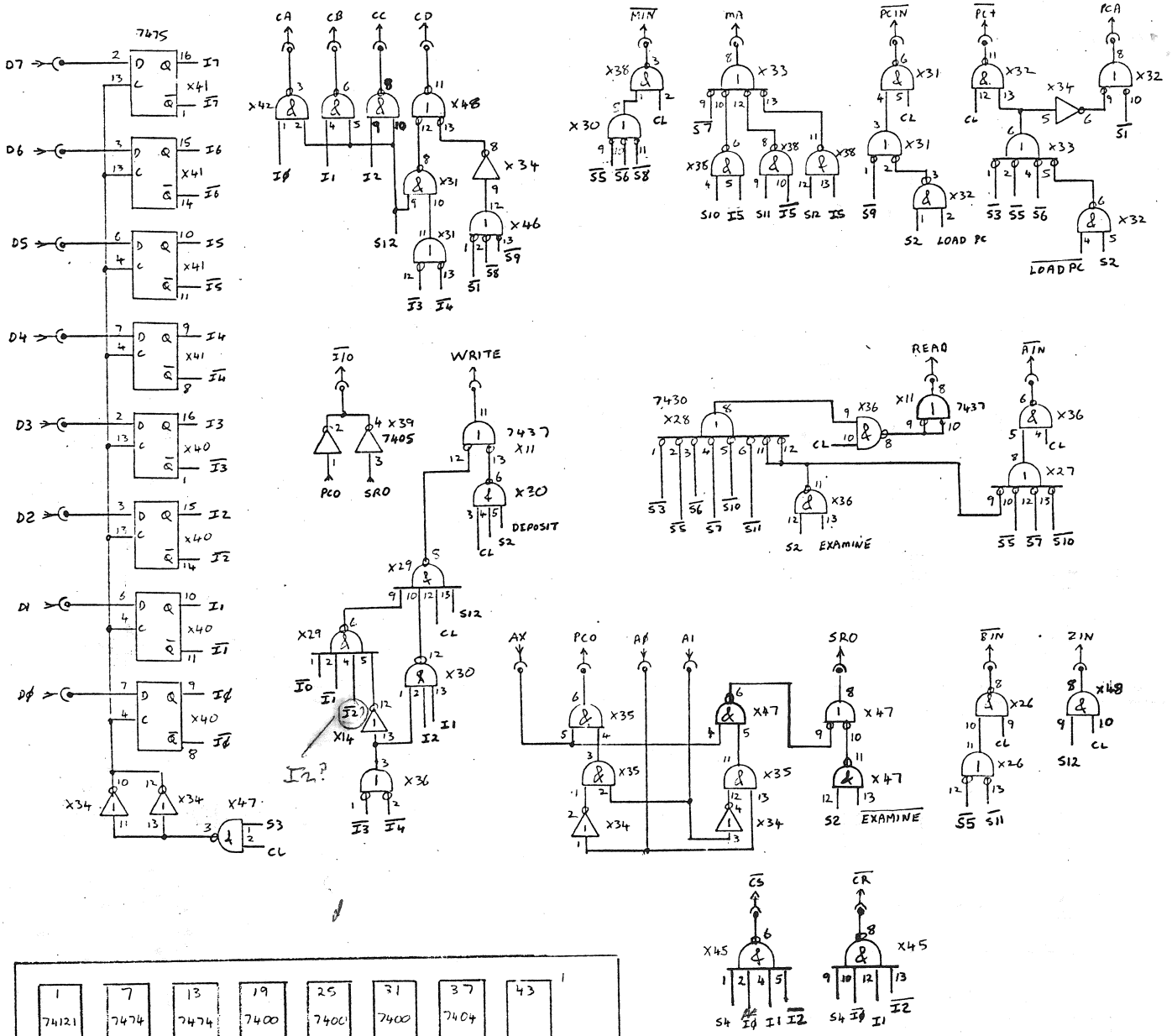
Sorry but have run out of space (and time); full testing details next issue.

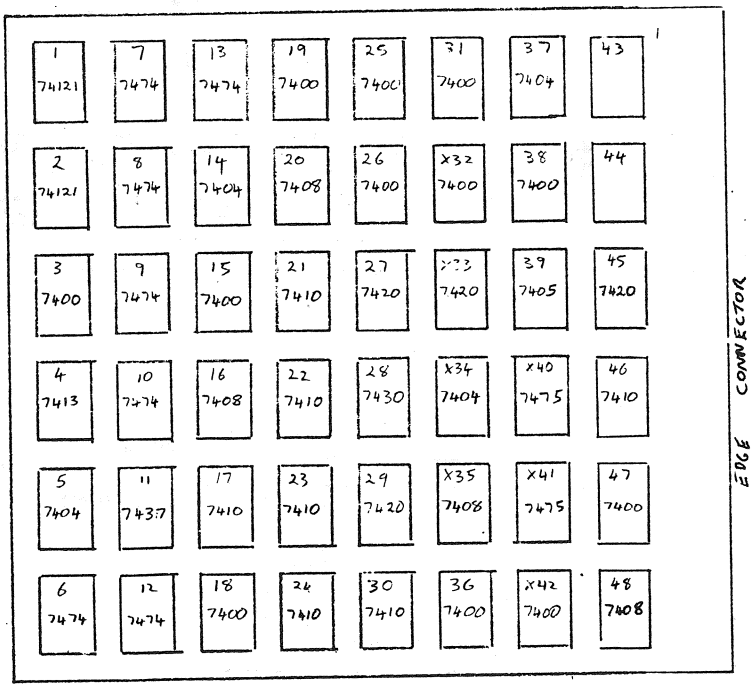


0V to pin 12 of X40,41
pin 7 all others

+5V to pin 5 of X 40,41
pin 14 all others



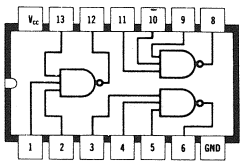




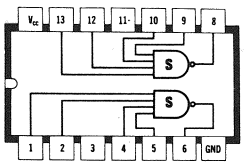
CONTROL UNIT PROPOSED LAYOUT

[X 43, 44 POSITIONS NOT USED]

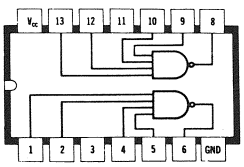
SN74 10N
Triple 3-input NAND gate



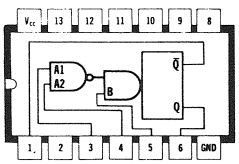
SN7413N
Dual 4-input NAND gate
Schmitt Trigger



SN74 20N
Dual 4-input NAND gate



SN74121N
Monostable multivibrator



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