Vol 1 Iss 1

ACCN

AMATEUR COMPUTER CLUB NEWSLETTER

March 1973

The Amateur Computer Club is open to all interested in the design, construction or programming of computers as a hobby.

For membership of the ACC and a subscription to Vol 1 of the ACCN (at least 4 issues), send 50p (75p for overseas members) to;

M.Lord
Amateur Computer Club
7 Dordells
Basildon, Essex

The Newsletter will appear every 2 or 3 months

And so the first issue of the ACCN comes out on the 25th anniversary of the invention of the transistor. An appropriate time, certainly without the transistor and the IC no amateur could hope to build even the simplest digital computer, and even commercial machines would be a rarity, accessible only to a select few initiated into the sacred arts & language and the ritual of hourly valve replacement.

From the letters received so far, it seems that about one half of our members are building or have completed a machine. The most ambitious plans are those of S.Panting, who is building "a fairly large machine with 10K 60 bit words of memory, TTY,VDU, mag tape, paper tape punch & reader attatched to a separate I/O unit with 4Kx16 memory - I am willing to supply information if & when completed and the bugs are ironed out ".

Many people are cautious about giving details of projects that are still in the constructional stage - don't be - even if you've only got the germ of an idea please pass it on to inspire others. In any case my own experience is that one never finishes, there is always some modification to do or some extra facility to be added.

I would like to publish full details of one machine in each issue, say a block schematic (down to the register level), instruction set, and any particularly interesting details of the system, construction or software.

THE SALE

The Electronic Hobbies Company grand closing sale in the caverns underneath St. Pancras station really was the sale to end all sales. In fact it may still be going on - see the advertisement in March Wireless World. I went down there on the first day and like everyone else there was staggered by the sheer amount of equipment and the low prices. The choice goodies took some searching out but in the end I got a good Friden Flexowriter and a sealed 4Kx20 core stack for a total of £19. (By the way, has anyone got any data on the Flexowriter ?). For anyone with a little more cash to spare and a large spare room there were two IBM 1401 processors and various assorted mag tape units, card punches & readers etc.

OLD COMPUTERS NEVER DIE . . .

Going to the sale led me to wonder what happens to all the old machines. Most digital computers seem to have a maximum useful life of about 10 years, or less if they are leased. Some do, of course, end up being sold as scrap or donated to the local school; but I suspect that a large number, especially those on lease, are just destroyed. This seems a terrible waste and surely there must be a way some of this 'junk' could be ligitemately diverted to peaceful amateur use. But how ?

Thinking along these lines - at the present time it is the first generation type of machine that is being scrapped, but in 5 - 10 years time ? Will we be resuscitating IBM 370 systems?

One group of enthusiasts in the USA have managed to get hold of 100 digital computers that were to have been scrapped when the Minuteman missiles were being re-furbished, together they have worked out the necessary modifications to convert them to general use.

ACCN FOR THE WIFE

Recruit a member today, with more members the cost of each copy of the ACCN goes down so we can publish more issues per volume.

DEVICES STRANGE

ROM's, RAM's, PROM's and now the WOM. Signetics have just brought out a 9046 bit random access Write Only Memory. Typical applications are said to include;

Don't care buffer stores
Artificial memory systems
First in - never out (FINO)
asynchronous buffers
Overflow Register (bit bucket)

INTEL MICRO COMPUTERS

The MCS-4 is a set of 4 MOS I/C's that can be combined to make a special purpose computer. They are;

The 4004 4 bit central processor unit. This consists of a 4 bit adder / shifter, 16 4 bit index registers, 4 12 bit program counters (3 of them being used as a 'return' address stack), an 8 bit instruction register and the control logic. The instruction set comprises 45 instructions including both binary and decimal arithmetic capability. As the set is intended for special purpose, dedicated, applications, the program is stored in 256 x 8 bit ROM's (the 4001) and data in the 4002 320 bit RAM - which also provides a 4 bit output port. Additional IO capability is provided by the 4003 10 bit serial shift register.

The 4004 itself provides all of the necessary control signals for 4Hx8 ROM, 1280x4 RAM and virtually unlimited I/O. The typical cycle time is 11 uS.

The 8008 is an 8 bit CPU that can be used with any type of memory. It contains an 8 bit accumulator, two 8 bit temporary registers, four flag bits and eight 14 bit address registers and the control logic. Cycle time is typically 20uS.

Intel have also developed two microcomputers using the 4004 and 9009, each on a single PC board. The SIM4-01 comes complete with one 4004, four 4002, TTY interface and clock generator. To avoid using the mask programmed 4001's, the board is equipped with the drive circuits and sockets for four 256x8 1701/2 electrically re-programmable ROM's.

The SIM8-01 uses the 8008 CPU with 1Kx8 RAM and sockets for 2Kx8 ROM - again the eraseable 1703. TTY interface and the clock generator are included on the 11.5 x 9.5 in board.

1972 prices for these devices (from Walmore Electronics Ltd. 11-15 Betterton St. London WC2H 9BS) were - for small quantities -

4002	£26.25	8008	£98.40
4003	5.30	4004	52.94
SIM4-01	£270.00		

THE GALDOR CENTRE

The following is taken from a handout sent by S.Fyfe;

"Who we are; Galdor is a group of interdisciplinary engineers and students who have bought themselves a second-hand computer and erected a building in which to operate it.

How we work ; The centre end the computer are made available for use by anyone at any time. Being an old computer (1960), depreciation is negligible and the centre is run 'at cost'.

Areas covered ; Work is encouraged from the student community and others in many fields including Sociology, Art, Ecology, Scientific, Survey Analysis etc. A minimum of commercial work makes the unit economically viable.

Advantages ; A free atmosphere, 'hands on' control of a powerful tool, advice and assistance and the general availability of information and help make such an 'alternative Processor' attractive.

Configuration ; It is an ICL 1301A with four ½" magnetic tape units, line printer 600 l/min, a card reader and punch, paper tape & full preparation equipment, 36 000 words of drum store and 2000 words of core store working with 48 bits per word and 12 uS fixed instruction time.

Developments ; The programming is well developed, and hardware enhancements are under way.

Action ; hard to beat as a democratic unit open to ideas. Drop round & see Galdor !

The Galdor Centre
52 Brighton Rd.
Surbiton, Surrey KT6 5PL
01 399 1300 "

SURPLUS BITS

J.Gray, Prospect House, Oakhill, Bath (0749 84 255) has a Shorts general purpose analogue computer for sale (or swap for a digital machine) . Details and parts list on request.

J.Florentin, 203/5 Old Marylebone Rd. London NW1 (01 262 6058 6-7pm Mondays, Thursdays or 01 589 5111 ext 2411 during working hours) writes; "If anyone would like to borrow a GPO 1200/600 baud modem they are very welcome. There are possibly more of these modems around that could be bought for £5-10 if anyone is interested. I have large no's of minature Jones and Belling Lee Unitor connectors for sale. I also have a grotty PT reader & punch £10 the pair. Also large amounts of low voltage PS components surplus to my requirements and an almost useable IBM model B but it has no IO switches or electromagnets, say £1 "

IBM 7090/4 & CDC 3000 code

0	000000	-	100000
1	000001	J	100001
2	000010	K	100010
3	000011	L	100011
4	000100	M	100100
5	000101	N	100101
6	000110	O	100110
7	000111	P	100111
8	001000	Q	101000
9	001001	R	101001
=	001011	$	101011
≠	001100	*	101100
+	010000		110000
A	010001	/	110001
B	010010	S	110010
C	010011	T	110011
D	010100	U	110100
E	010101	V	110101
F	010110	W	110110
G	010111	X	110111
H	011000	Y	111000
I	011001	Z	111001
.	011011	,	111011
)	011100	(	111100

(≠ - on IBM 7090/4)

Digital Computer — ULO 510 — I.D.Spencer

10 bit words (2 five bit characters / word). Max 8K memory which can be of any type as the CPU treats memory as a special peripheral and can accept any cycle time. 2's complement arithmetic. Standard interrupt structure (priority by software).

Hardware registers;

P register is the program counter (13 bits)
MAD is the memory address register (13 bits)
SR is the sector register (3 bits)
GPR is the group register (5 bits)
M is the memory data register (10 bits)
F is the function register (5 bits)
A is the primary data register (10 bits)
B is the secondary data register (10 bits)
O is the operator's register (10 bits)
(The adder is a one bit serial adder, the P register is wired as a counter. The A,B,M,O,GPR & SR are shift registers)

Memory is divided into sectors of 1024 locations each, and each sector is divided into 32 groups of 32 locations each.

Memory Reference Instructions;

LDA loads the A reg with the contents of the specified location.
STA stores the A reg in the specified location.
ADD adds the content of the specified location to the A reg.
CAS compares the content of the specified location with the A reg, if A is the larger then execute the next instruction, if they are equal skip one instruction, if A is the smaller skip two instructions.

JMP unconditional jump to the specified location
JST jump and store program count
IRS increment specified location, if zero skip one instruction

I/O instructions;
OCP device control instruction
INA input to A reg from device
OTA output from A to device
SNS sense test instruction
All I/O instr skip if successful

SKP instructions, skip if;

A is zero	A is not zero
A bit 1 is 0	A bit 10 is 0
B bit 1 is 0	B bit 10 is 0
Sense sw set	Sense sw not set

AAD instructions;
TCA 2's complement A
TCB 2's complement B
APB A plus B
AMB A minus B
BMA B minus A
AOA add 1 to A
AOB add 1 to B
note... result always goes to A reg

ORA instructions;
LOA operators reg to A
IOA interchange operators reg and A
LOB operators reg to B
IOB interchange operators reg and B
note... these instr available with test for O reg loaded and skip if successful, and ability to set operator request light for data in O reg if test fails.

SFT instructions (all right shift);
Shift A Shift B
Shift A & B together
Shift A & B independantly

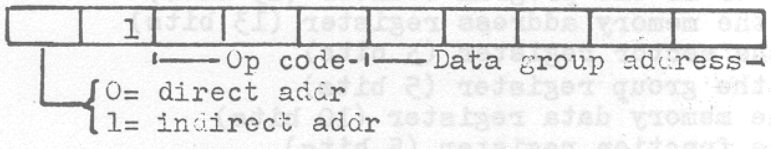
ROT instructions;
Rotate A Rotate B
Rotate A & B together
Rotate A & B independantly

CLR instructions;
CLA set A reg to zero
CLB set B reg to zero
SGP set GPR to 11111
SCB set C bit (adder carry bit) to 1
RCB reset C bit

GEN instructions;
ENB enable interrupt
INH inhibit interrupt
HLT halt
ISG input SR & GPR to A reg
NSR normalise sector reg (SR)
IND independant B shift & rotate
note .. all of these instr (except HLT) may be executed at the same time. The ISG instr inputs SR & GPR to A along with op code for special LSG instr (for execution later)

LSG instruction;
loads sector and group addresses for use by program

Memory Reference;



As can be seen only 5 bits are available for addressing (plus one bit for indirect addressing). A memory ref instruction normally refers to an address in the group of locations referred to by the GPR register (in the same sector as the instruction). The contents of the GPR can be changed with the LSG instruction. This group of locations is known as the DATA GROUP.

The normal data group for a sector is the highest group in the sector '37. Locations o,1,2,3 of the data group can hold data in the normal way but if they are indirectly addressed they themselves become indirect addresses (used for multilevel indirect addressing).

Other locations in the data group hold either data or addresses and as they are 10 bits long may refer to any location in the sector ahen read as an indirect address.

Note .. JMP instructions refer to locations in the instruction group referred to by the P register, not the GPR, but indirect JMP refers to locations in the data group.

To allow the program to move from sector to sector for data addresses or instructions the SR register is utilised. Normally The SR holds the same sector address as the P register but it can be changed with the LSG instruction. If the SR specifies a different sector to the P reg direct addressing is treated normally but indirect addressing in a mem ref instruction causes not indirect address but the hardware to go to the address specified by the instruaction in the SR sector instead of the same sector. If a JMP instruction is performed in this way the P reg will end up containing the same sector as the SR and the program then continues normally. The SR can be normalised to the same sector as the P reg by means of the NSR instruction.

Data words are 10 bits long, bit 1 (MSB) specifies the sign of the word giving a range of +511 to -512. However the comprehensive shift instructions make double precision by software fairly economical which gives the machine a basic double precision modular range of + 524287 to -524288.

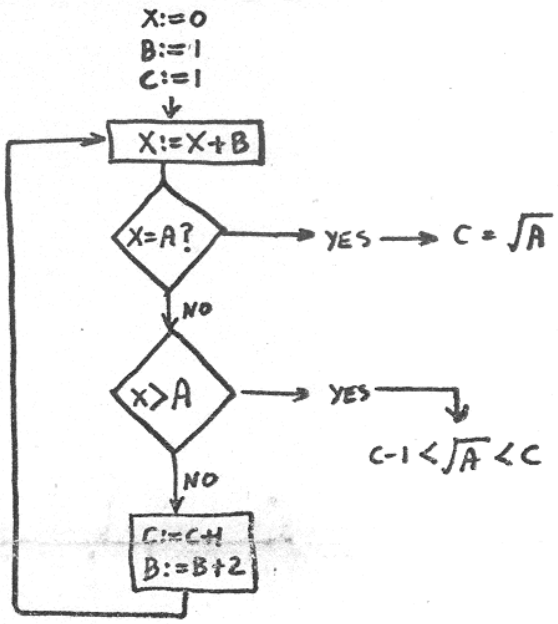
Normal input and output via a modified Creed teletype using a modified 5 bit Murray code. It is of course eventually hoped to expand the machine to incorporate mag tape and some real time interfacing.I would also like to carry out some development on basic time sharing and communication using the machine.

The CPU has three basic cycles of operation; Fetch, Indirect & Execute. Each cycle is made up of a number of timing levels between TLo and TL7, not all cycles will have all of these timing levels and exit to a new cycle can take place from a number of different timing levels.

The memory is treated as a peripheral (but not the same as an IO peripheral) of the CPU and while locations are being accessed the CPU is stalled by a MEMWAIT signal. Also, while registers are being shifted under contral of a shift counter the CPU timing levels are stalled

SQUARE ROOT ALGORITHM

To find the approximate square root of A (A greater than 1)



and of course the answer can be made more accurate by scaling, i.e. multiply A by 100, then divide the answer by 10.